* Counter-type A/D Converter:

- One of direct type ADCs

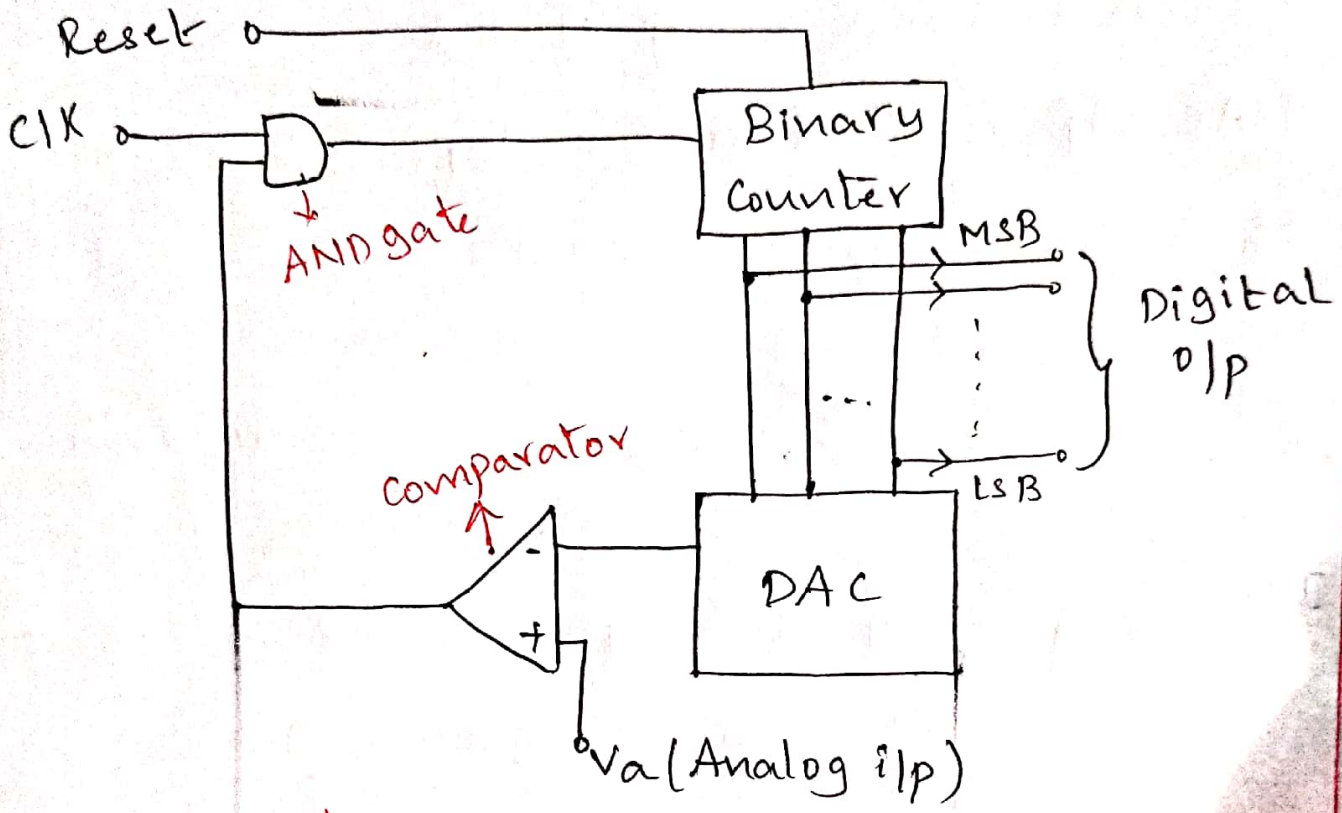


Fig: Counter-type A/D Converter

Fig Description: CKT Comprises of

- N-bit Binary Counter (with Reset control signal)
- DAC
- comparator
- AND gate

→ Comparator o/p

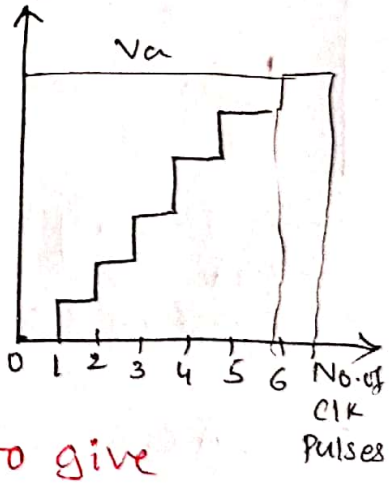
$V_a > V_d$ → 1 → Counting starts

$V_a \leq V_d$ → 0 → Counting stops

Working Principle:

- The counter is reset to zero count by reset pulse.
- Upon release of RESET, the clock pulses are counted by binary counter

- Clock pulses go through AND gate;
- No. of clk pulses counted increase with time.
- This count will be represented in binary word, which is used as i/p of DAC
- DAC o/p is a staircase type
- If $V_a > V_d$ → o/p of comparator becomes high
  ↳ AND gate is enabled
    ↳ Allows the transmission of the clock pulses to the counter
- If $V_a \leq V_d$ → o/p of comparator becomes low.
  ↳ AND gate is disabled
    ↳ counting stops.
- For a new value of analog i/p Va, a second reset pulse is applied to clear the counter.



- Counter freq must be low enough to give sufficient time for the DAC to settle & for the comparator to respond.
- Drawback of this method ⇝ LOW SPEED.
  ↳ Conversion time can be as long as $(2^n - 1)$ clk ~~pulses~~ periods depending on the magnitude of i/p voltage Va
- If analog i/p voltage varies with time, the i/p signal is sampled, using a sample & hold ckt before it is applied to comparator.

* Successive Approximation Converter: (Roy choudary) (10.3.4)

- Uses a very efficient code
- ✱ Completes n-bit Conversion in just n-clock pulses / Periods ✱
- Fig 10.13 shows 8-bit Converter

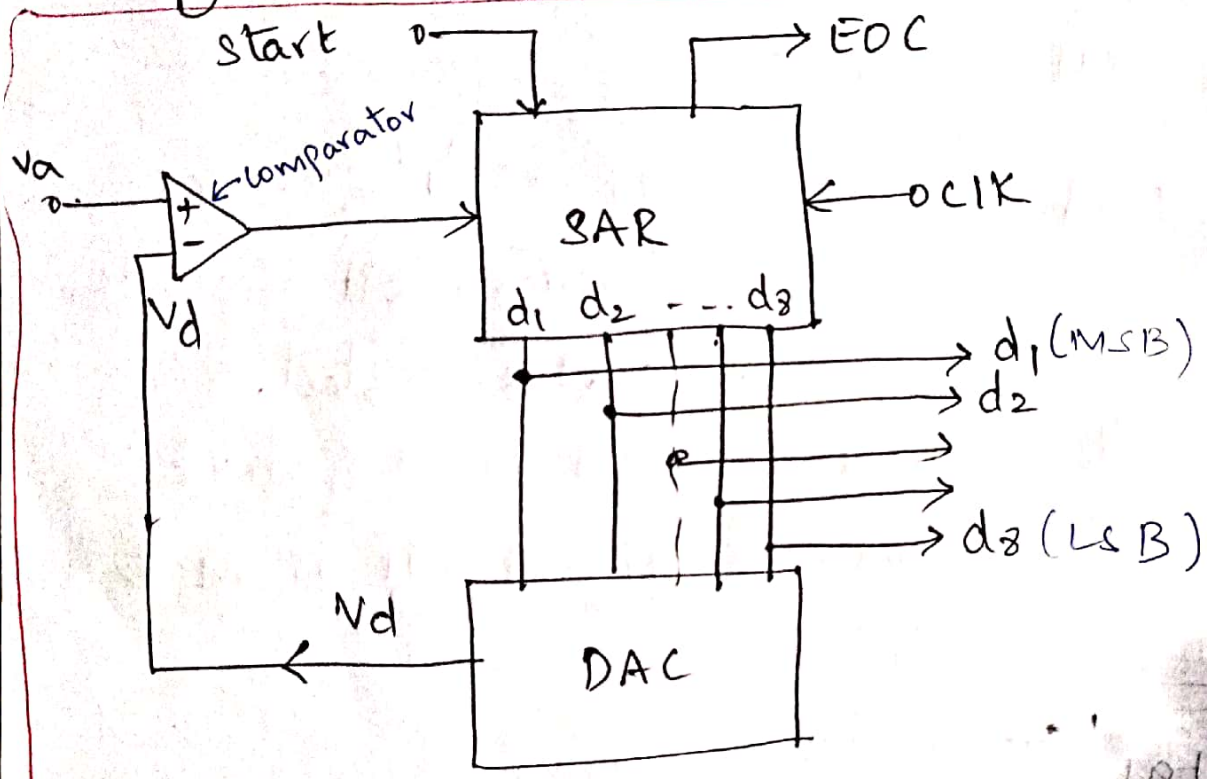


Fig: Functional diagram of the successive approximation ADC

{ SAR → Successive Approximation Register

~~Working operation~~:

Description of Fig: CKt comprises of

- an op-amp Compator
- SAR (with start, EOC & clk)
- DAC

comparator o/p
$V_a > V_d$ → logic 1
$V_a < V_d$ → logic 0

Working Principle:

→ With the arrival of the START command, SAR sets MSB $d_1 = 1$ with all other bits to Zero so that the trial code is 10000000.

→ O/p of DAC is V_d; it is compared with i/p analog voltage V_a.

→ If $V_a > V_d$ → MSB is left at '1' & next lower significant bit is made '1' and further tested.

→ If $V_a < V_b$ → MSB is reset to '0' & next lower significant bit is made '1'

Correct digital representation	Successive approximation register o/p V_d at different stages in the conversion	Comparator o/p
11010100 (212.5 V) ± ½ (LSB)	10000000 (128 V) $V_a > V_d$	1
	11000000 (192 V) $V_a > V_d$	1
	11100000 (224 V) $V_a < V_d$	0
	11010000 (208 V) $V_a > V_d$	1
	11011000 (216 V) $V_a < V_d$	0
	11010100 (212 V) $V_a > V_d$	1
	11010110 (214 V) $V_a < V_d$	0
	11010101 (213 V) $V_a < V_d$	0
	11010100	

Advantages of this technique:

- Here Conversion time is independent of the i/p voltage
- High accuracy
- Easy to use
- Low power consumption

* Dual-slope ADC / Integrating type ADC:

- This type of ADC do not require S/H CKt at i/p.

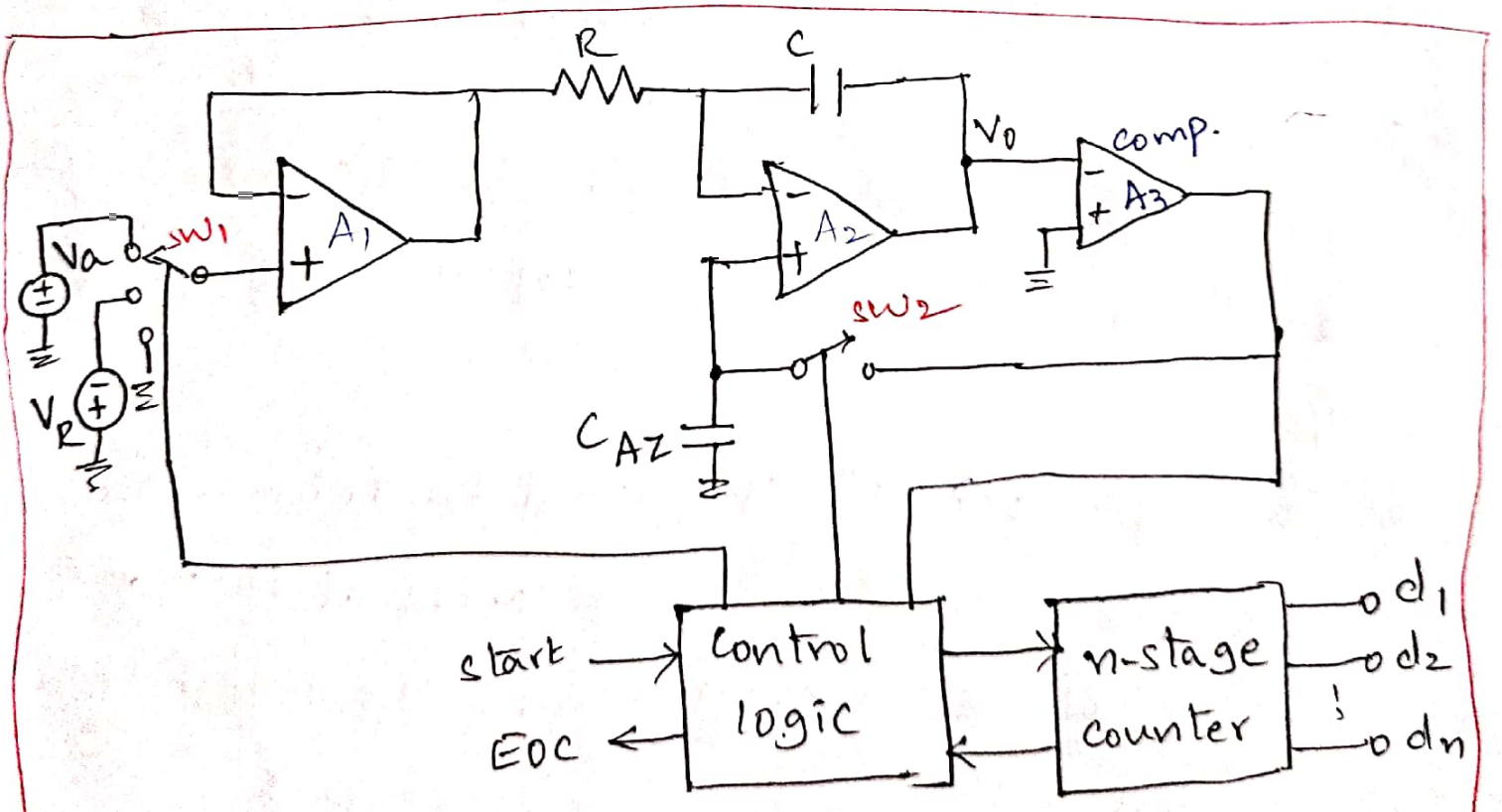


Fig: Functional diagram of dual slope ADC

(1)

Fig. Description : CKt Consists of

- 3 op-amps → A_1 → buffer of high i/p imp.
  - → A_2 → Integrator
  - → A_3 → Comparator
- n-stage counter ⇝ Ripple counter
- Control logic ⇝ START, EOC & CLK

~~Working Principle~~:

NOTE: → In this ADC, first analog i/p signal V_a is integrated for a fixed duration of 2^n clock periods.

→ Then it integrates an internal reference voltage V_R of opposite polarity until the integrator o/p is zero.

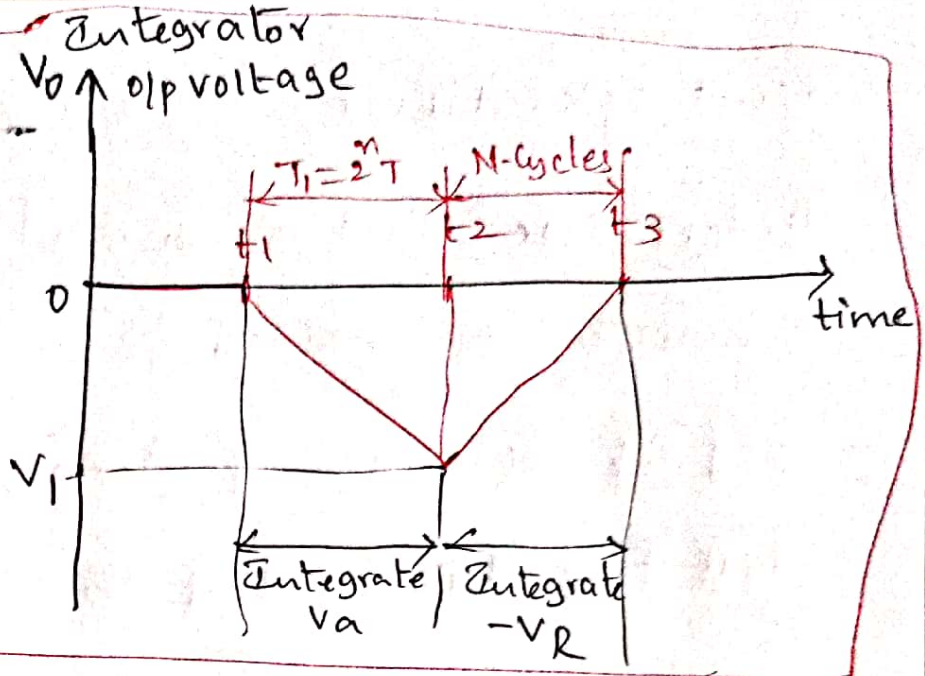
→ No. of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period

→ N represents the desired o/p code

Circuit operation:

- Before the "start" command arrives, SW_1 is connected to ground & SW_2 is closed.
- Offset voltages of A_1, A_2 & A_3 appears across ~~are stored in~~ C_{AZ} till the threshold of the comparator is achieved
- Thus C_{AZ} provides automatic compensation for the i/p-offset voltages of all the three amplifiers.
- When SW_2 opens → C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.
- At the arrival of START command at $t=t_1$,
  - ↳ control logic opens SW_2 & SW_1 connects to V_a and enables the counter starting from zero.
- Counter resets to zero after counting 2^n pulses.
- If T is the clock period, integration takes place for a time $T_1 = 2^n \times T$ & the o/p is a ramp going ~~downward~~ downwards as shown in fig

* Dual slope ADC :-



② Fig: Integrated o/p waveform for dual slope ADC

- At end of interval ~~Fig~~ T_1, counter resets itself to zero & SW_1 is connected to Ref voltage $(-V_R)$.
- Now, o/p voltage V_0 will have a positive slope
- As long as V_0 is negative, o/p of comparator is positive & Control logic allows the clock pulse to be counted.
- When V_0 becomes just zero at $t = t_3$, Control logic issues an end of Conversion (EOC) command And no further clock pulses enter the counter
- It can be shown that the reading of the counter at t_3 is proportional to analog i/p voltage V_a.

From Fig ②,

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

and $$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

For an integrator, $V_o = \frac{-1}{RC}\int V_i(t)$ (o/p ↙, V_i i/p)

Here, $$\Delta V_o = \frac{-1}{RC} V(\Delta t)$$

→ At instant t_2, $V_o = V_1$

Above eq → ∴ $$V_1 = \frac{-1}{RC} V_a (t_2 - t_1) \quad -(1)$$

→ Also, V_1 is given by

$$V_1 = \frac{-1}{RC} (-V_R)(t_2 - t_3) \quad -(2)$$

Equating eqs. ① & ②

$$V_a(t_2 - t_1) = -V_R(t_2 - t_3)$$

$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

∵ $t_2 - t_1 = 2^n$ & $t_3 - t_2 = N$

∴ $$V_a(2^n) = V_R(N)$$

$$\boxed{V_a = V_R\left(\frac{N}{2^n}\right)}$$

N → digital count

n → n in stage counter

NOTE:

- Since V_R & n are Const, $\boxed{V_a \propto N}$

  V_a → analog i/p voltage

  N → count reading

  V_a ⇝ independent of R, C & T

- Advantage of dual-slope ADC:

  ↳ Dual-slope ADC integrates the i/p signal for a fixed time, hence it provides excellent noise rejection of Ac signals, whose periods are integral multiples of integration time T_1.

  ↳ Dual-slope converters are suitable for accurate measurement of slowly varying signals, such as thermocouples & weighing scales.

Disadvantage:

↳ long Conversion time