* Sample-And-Hold:

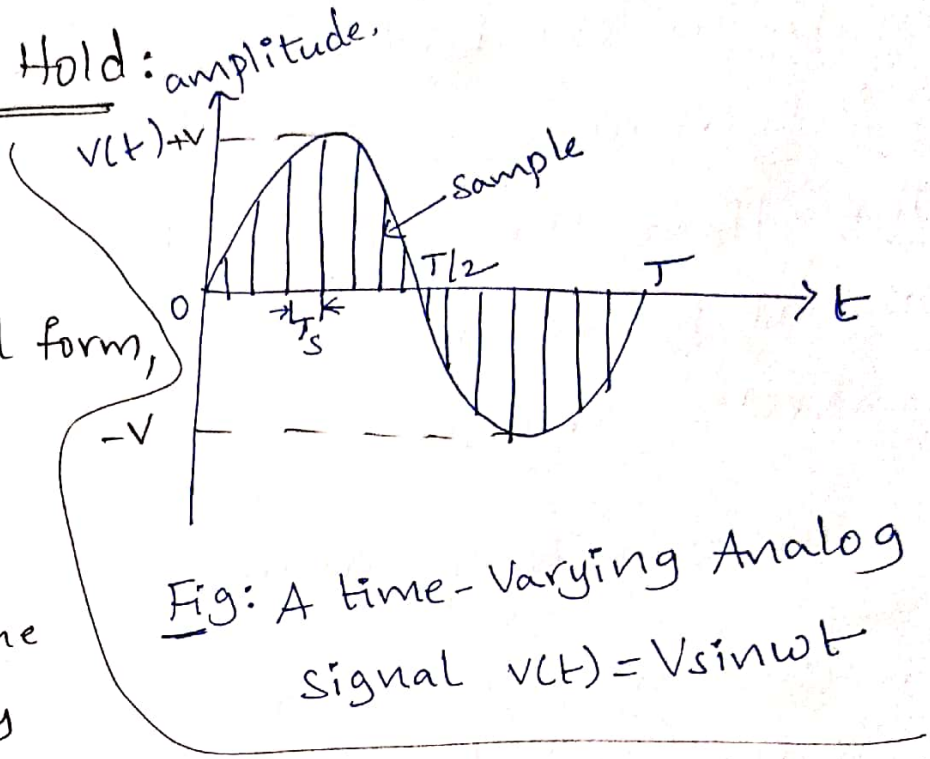


Fig: A time-varying Analog signal $V(t) = V\sin\omega t$

- TO convert this signal into digital form, we have two ways.

(1) The value of the signal at every instant of time is required to be converted into a group of 'n' no. of bits.

→ This process will yield an infinite no. of analog voltage values & thus is not at all practicable

(2) TO take samples of V(t) at regular intervals, ie; signal is sampled regularly every T_s.

→ Then according to sampling theorem, the signal can be uniquely determined & reconstructed from these samples with no error

→ Time T_s → sampling time & $f_s = \frac{1}{T_s}$ → sampling rate

→ According to sampling theorem, $f_s \geq 2f$ where f → frequency of the analog signal.

- The constant voltage corresponding to each sample is obtained using a sample-and-hold (S/H) circuit
- The o/p of the S/H circuit is converted to digital signal by means of an analog-to-digital (A/D) converter circuit.

Sample-and-Hold Circuit:

- In this circuit, voltage across the capacitor follows the i/p signal voltage V_i → when S is closed.

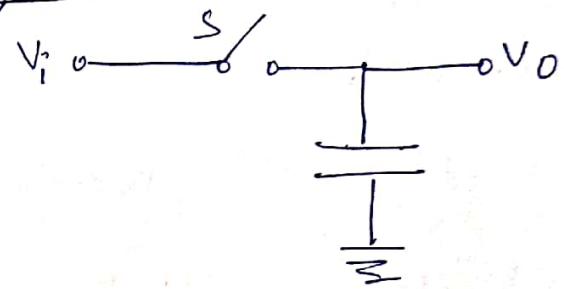


Fig: Basic sample-and-Hold circuit

Sample and Hold ckt samples the i/p signal and holds on to its last sampled value until the i/p is sampled again

- When S is open → capacitor holds the instantaneous value of the signal voltage attained just before S is opened
- Thus for every T_s, switch is closed for a short duration & then opened.

- The dc voltage across the capacitor gives the value of the signal at the instant the switch is opened
- The dc voltage represents a sample of the signal & is converted to digital signal using A/D converter ckt

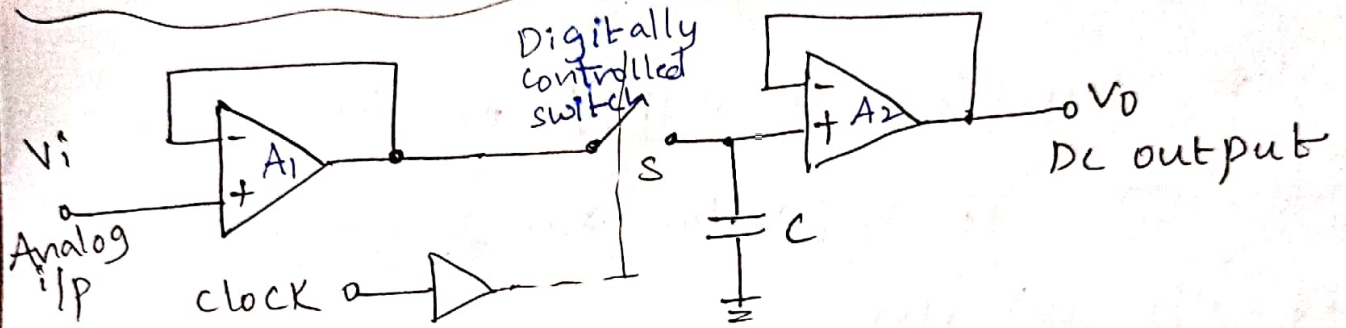


Fig: A practical sample-and-Hold circuit

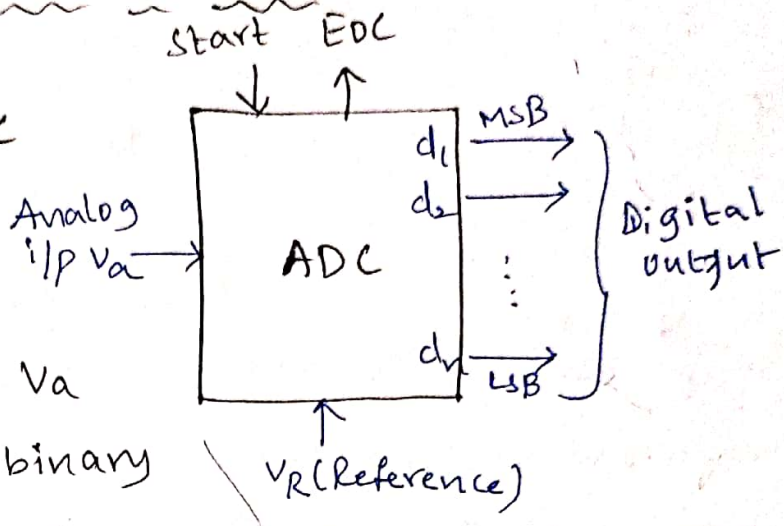
- Fig consists of two unity gain amplifiers A_1 and A_2 and a digitally controlled switch S.
- Analog i/p voltage is applied at the i/p of buffer amplifier A_1.
- These (op-Amps) amplifiers have high i/p impedances & low o/p impedances.
- The high i/p impedance of A_1 will prevent loading of the analog signal & its low o/p imp. will help in fast charging of the capacitor C when S is closed.

- Switch is controlled by a clock generator which makes the switch operate at regular intervals as required according to the sampling rate.
- The voltage across the capacitor is applied at the i/p of the analog-to-digital converter through buffer amplifier A_2.
- Here, the high i/p imp. of A_2 avoids discharge of capacitor due to loading effect of A/D converter.
- Accuracy of the ckt depends upon the holding of the charge in the capacitor.
- Therefore, a capacitor with a very low leakage must be used.
- A capacitor with polycarbonate, polyethylene or Teflon dielectric is prefered.

* Functional diagram of ADC:

or

Schematic of ADC



- It accepts an analog i/p voltage Va & produces an o/p binary word $d_1 d_2 \cdots d_n$ of functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}.$$

where $d_1 \rightarrow$ MSB ; $d_n \rightarrow$ LSB.

- An ADC usually has two additional control lines :
  - START → i/p to tell ADC when to start conversion
  - EOC → o/p to tell when to end conversion
- Depending upon type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

Types of ADCs:

- **Direct type ADCs**
  - compares given analog signal with internally generated equivalent signal
    - Flash (comparator) type converter
    - Counter type converter
    - Tracking (servo) converter
    - Successive approximation type converter
- **Integrating type ADCs**
  - conversion takes place indirect manner
    - changes the given analog signal to a linear fn. of time/freq & then to a digital code
      - charge balancing ADC
      - Dual-slope ADC

- Most commonly used ADCs are successive approximation and the integrator type

* Quantization and Encoding:

- In D/A converter, possible no. of digits i/ps is fixed.
  EX: In a 3-bit D/A converter, there are 8 possibl i/ps.
- In contrast, ~~the~~ in A/D converter, the i/p analog voltage can have any value in a range, but the digital o/p can have only 2^N discrete values for n-bit A/D converter.
- Therefore, the whole range of analog voltage is required to be represented suitably in 2^N intervals. This process is known as Quantization
- Each interval is then assigned a unique N-bit binary code, which is referred to as encoding

Example: Consider an analog voltage in the range of 0 to V and a 3-bit digital o/p for any in the range

↳ lets divide whole range in 8 intervals with size $s = V/8$.

↳ Each interval is assigned a 3-bit binary value

Analog Voltage	Equivalent digital value.
V	111
7/8 V	110
6/8 V	101
5/8 V	100
4/8 V	011
3/8 V	010
2/8 V	001
1/8 V	000
0	

Fig: Quantization & Encoding

→ we can observe that the whole range of voltage in an interval is represented by only one digital value

→ i.e) if given i/p voltage is in the range 0 to 1/8 V, 000 will be the represented digital value

↳ This leads to the error in the Conversion process, which is called Quantization error

→ Quantization error can be reduced if the size of
  ↳ top & bottom intervals as S/2
  ↳ middle six intervals as S
  } is assumed

→ Quantization error can also be specified in terms of LSB.
  ↳ Max. quantization error is $\pm \frac{1}{2}$ LSB.

---

* Parallel-comparator A/D converter:

- Also called as Flash A/D converter
- Simplest, possible A/D converter, fastest
- Expensive technique

- Fig shows a 3-bit A/D converter

Fig Description: circuit comprises of
- a resistive divider n/w
- 7 op-amp comparators
- latches
- Decoder
- i/p to the ckt is V_a as Analog voltage
- V → Reference voltage
  ↳ Full scale voltage

Working:

- At each node of the resistive divider, a comparison voltage is available

Voltage i/p	logic o/p C
$V_a > V_d$	1
$V_a < V_d$	0
$V_a = V_d$	Previous value

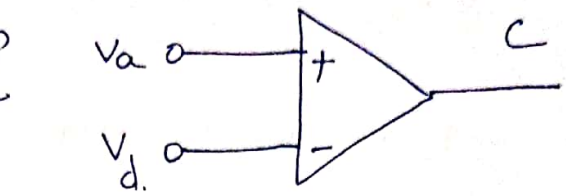


Fig. 10.19, Table 10.6

Advantage of this ADC (A/D converter):

↳ provides high speed conversion; fastest
  ↳ conversion time is 100ns or less.

Disadvantage of this ADC (A/D converter):

↳ No. of comparators approximately doubles for each added bit
  ↳ In general, for n-bit converter, $(2^n - 1)$ comparators are required

Ex: A 2-bit ADC requires 3 comparators.

3 " " 7 "

4 " " 15 ".