CHAPTER 10

D-A And A-D Converters

10.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 10.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

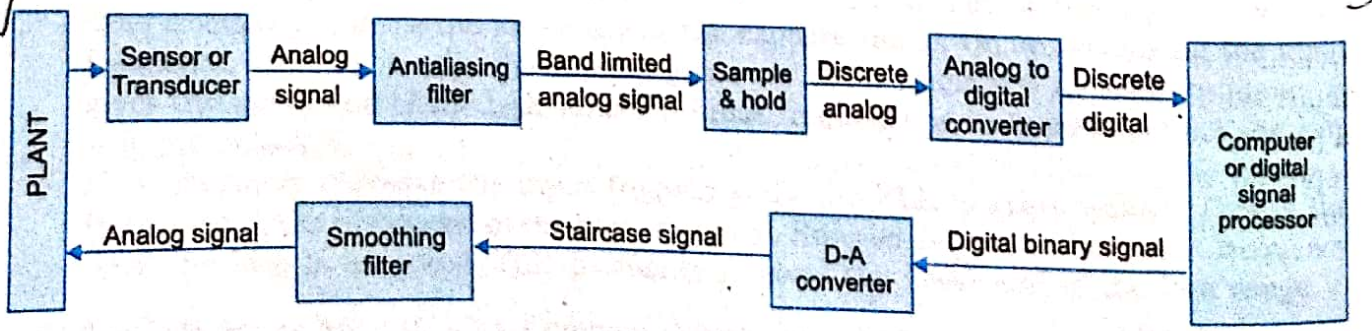

Fig. 10.1 Circuit showing application of A/D and D/A converter

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The scheme given in Fig. 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

10.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 10.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

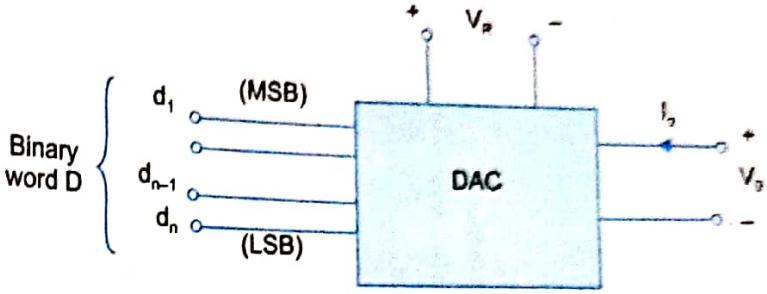

Fig. 10.2 Schematic of a DAC

$$V_o = K\, V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad (10.1)$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

There are various ways to implement Eq. (10.1). Here we shall discuss the following resistive techniques only:

Weighted resistor DAC

R-2R ladder

Inverted R-2R ladder

10.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 10.3(a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 10.3(a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

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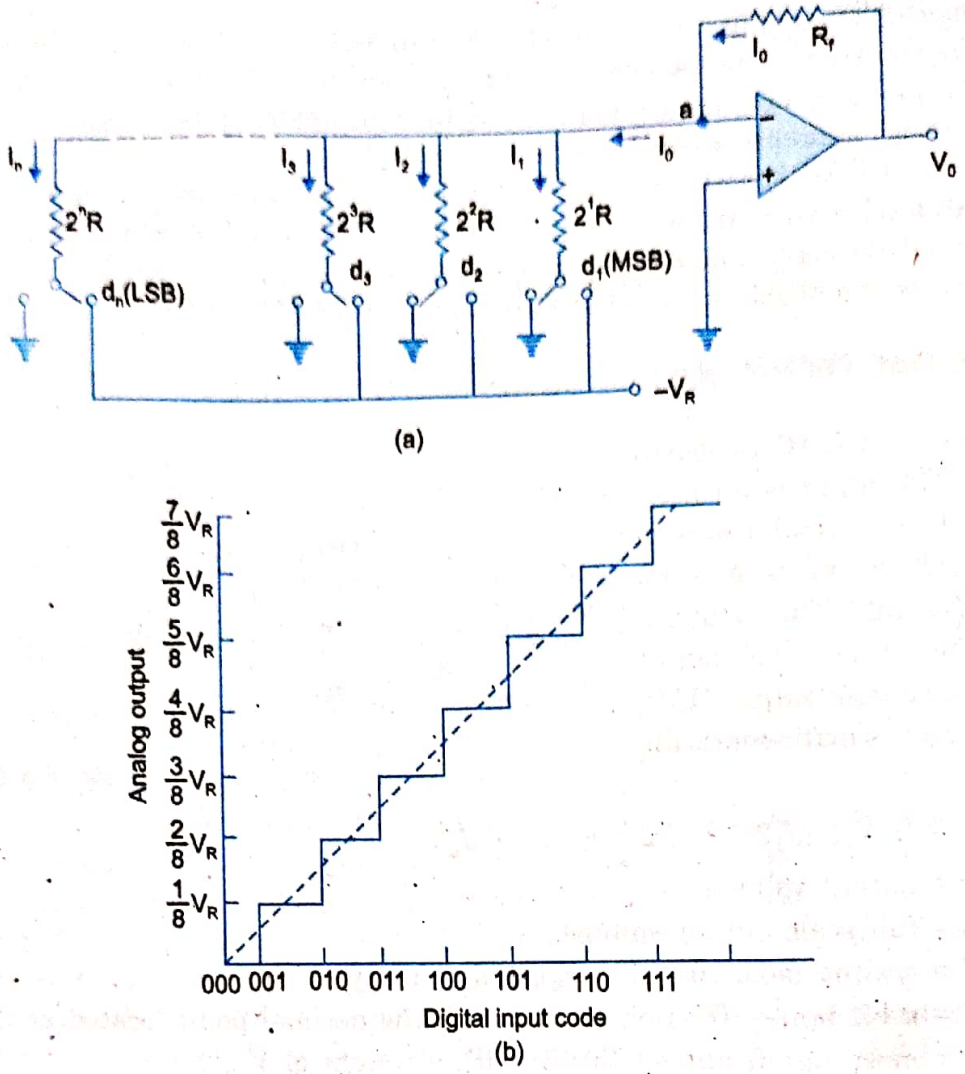

Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

$$= \frac{V_R}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad (10.2)$$

Comparing Eq. (10.1) with Eq. (10.2), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 10.3(a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 10.3(b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 10.3(a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be + 5 V and the output will be negative.

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The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 10.3 (a) are in series with resistors and therefore, their *on* resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of digitally controlled SPDT electronic switches are available of which two are shown in Fig. 10.4. A totem-pole MOSFET driver in Fig. 10.4(a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 10.3(a). The two complementary gate inputs Q and $\overline{Q}$ come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to – 10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\overline{Q} = 0$. This drives the transistor Q_1 *on*, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains *off*. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 10.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5$ V and $V(0) = 0$ V. The complement $\overline{Q}$ of the bit under consideration is applied at the input. Thus $\overline{Q} = 0$ makes transistor Q_1 *off* and Q_2 *on*. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\overline{Q} = 1$ the output of the CMOS inverter is 0V connecting the resistance R_1 to ground.

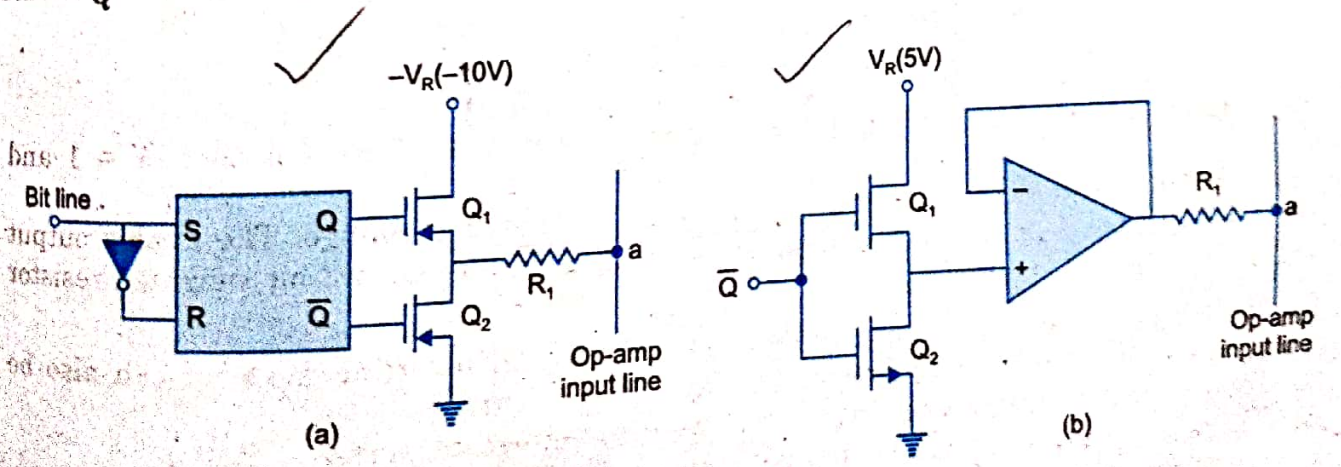

Fig. 10.4 (a) A totem pole MOSFET switch (b) CMOS inverter as switch

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10.2.2 R-2R Ladder DAC

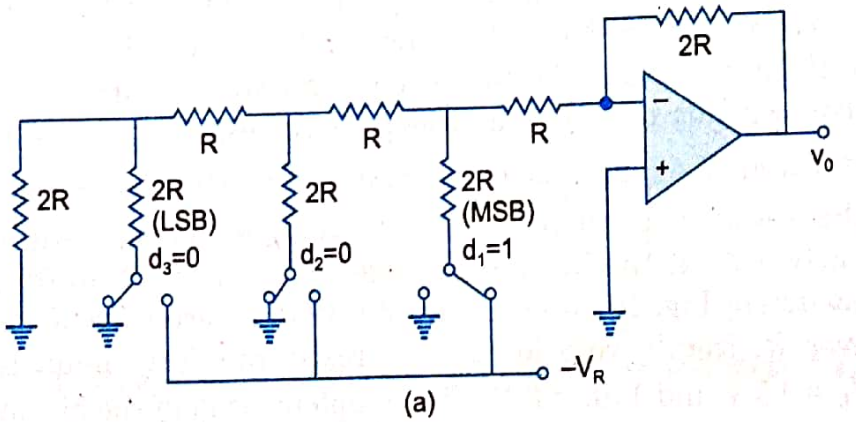
Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

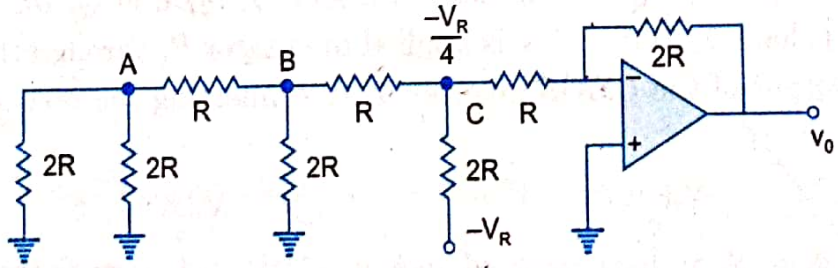
$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$



(a)



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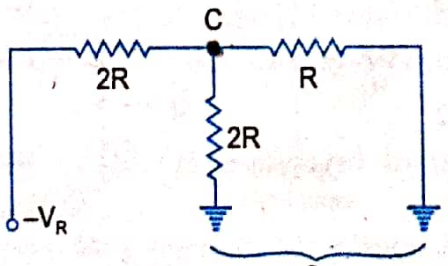

(c)

Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

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The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 10.6 (a). The circuit can be simplified to the equivalent form of Fig. 10.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

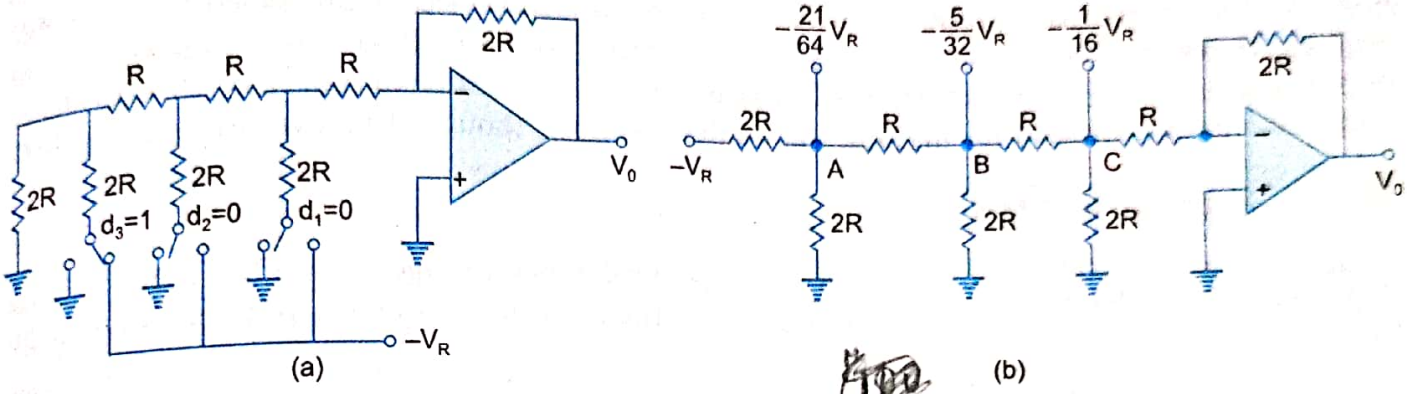

Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

10.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 10.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 10.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 10.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current

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mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 10.7(a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 10.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 10.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

10.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (10.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then,

$$v_0(t) = V_{om} \cos (2\pi ft + 180°)$$

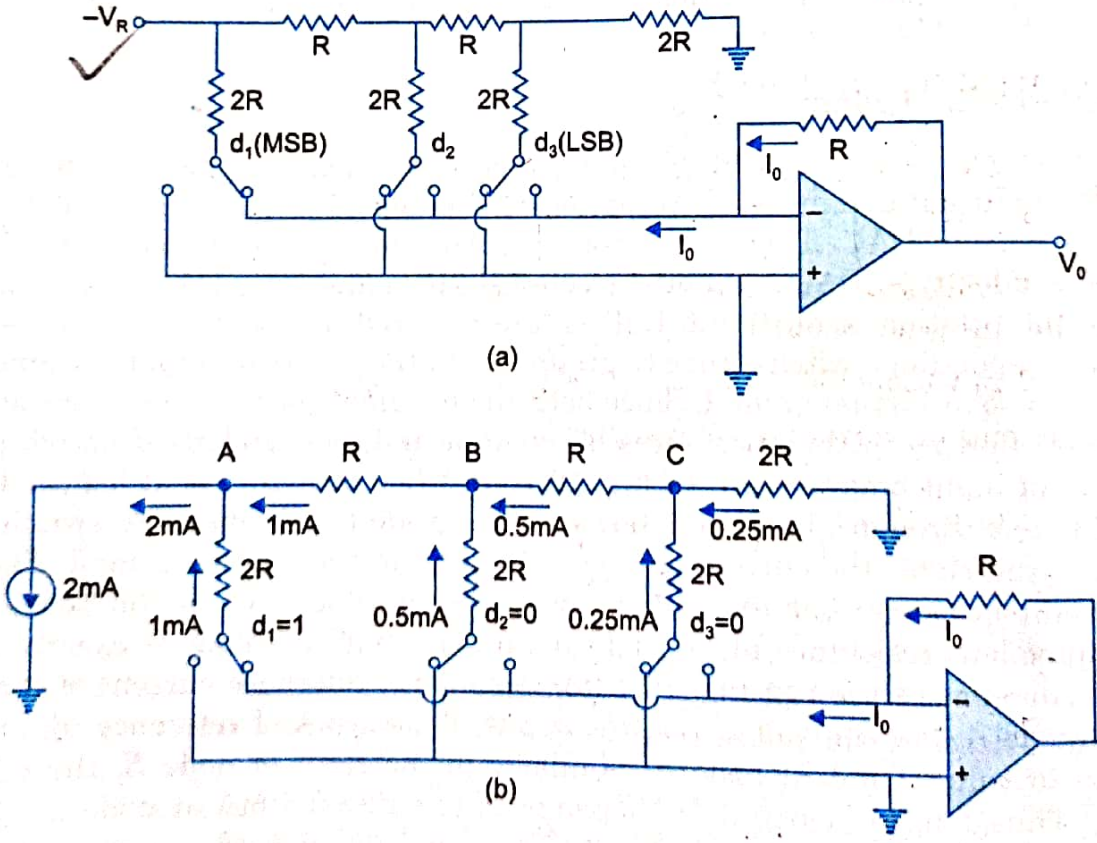

Fig. 10.7 (a) Inverted R-2R ladder DAC (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

where V_{om} will vary from 0V to $(1-2^{-n})\ V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a

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fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

10.2.5 Monolithic DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 10.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{cc} = + 5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current source is determined by resistor R_{14} and voltage reference V_R and is equal to V_R/R_{14} = 5V/2.5 kΩ = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^{8} d_i \, 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through d_1 = 1)

$$I_o = \frac{5\text{ V}}{2.5\text{ k}\Omega} \left(\sum_{i=1}^{8} 1 \times 2^{-i} \right) = 2 \text{ mA } (255/256) = 1.992 \text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2 \text{ mA } (255/256) \times 5 \text{ k}\Omega = 9.961 \text{ V}$$

In general, the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from – 5 V to + 5 V by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 10.8 (b). The resistor R_B supplies 1 mA (= V_R/R_B) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14}) \left(\sum_{i=1}^{8} d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I_o' R_f = (I_o - V_R/R_B) R_f = (0 - 5 \text{ V}/5 \text{ k}\Omega) \times 5 \text{ k}\Omega = -5 \text{ V}$$

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For binary input word = 10000000, output V_o becomes

$$V_o = (I_o - V_R/R_B)R_f = [V_R/R_{14})\ (d_1/2) - (V_R/R_B)]R_f$$
$$= [(5\ V/2.5\ k\Omega)\ (1/2) - (5\ V/5\ k\Omega)]\ 5\ k\Omega = (1\ mA - 1\ mA) \times 5\ k\Omega = 0V$$

For binary input word = 11111111, output V_o becomes

$$V_o = [(V_R/R_{14})\ (255/256) - (V_R/R_B)]R_f = (1.992\ mA - 1\ mA) \times 5\ k\Omega$$
$$= 0.992\ mA \times 5\ k\Omega = +4.960\ V$$

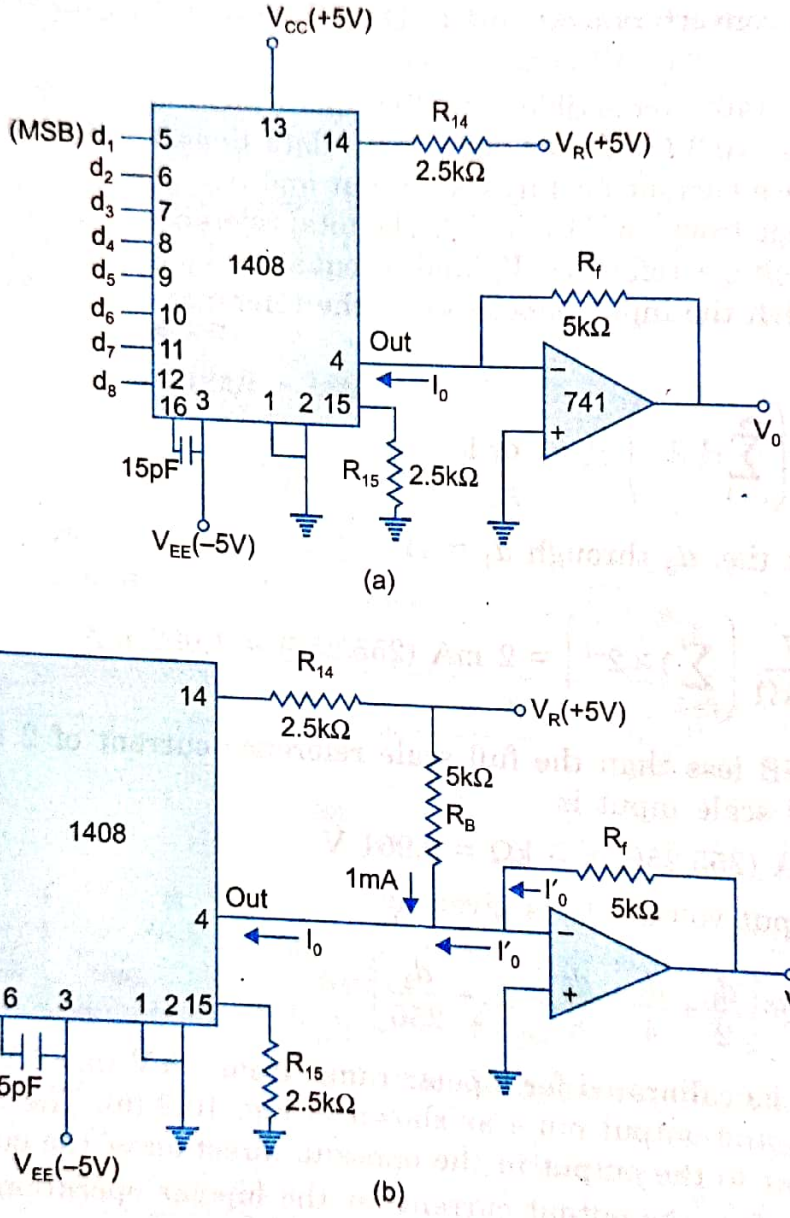

Fig. 10.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 10.1

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

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Solution

The output voltage for input 101101111 is
$= 10.3 \text{ mV } (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$
$= 10.3 \text{ mV } (367) = 3.78 \text{ V}$

Example 10.2

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $\text{LSB} = \frac{10 \text{ V}}{256} = 39 \text{ mV}$

and $\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5 \text{ V}$

Full scale output = (Full scale voltage − 1 LSB)
= 10 V − 0.039 V = 9.961 V

Example 10.3

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2-bit D/A converter)
(ii) 0110 (for a 4-bit DAC)
(iii) 10111100 (for a 8-bit DAC)

Solution

(i) $V_o = 10 \text{ V}\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5 \text{ V}$

(ii) $V_o = 10 \text{ V}\left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75 \text{ V}$

(iii) $V_o = 10 \text{ V } (1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$
$= 10 \text{ V } (1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34 \text{ V}$

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10.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution: The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8-1 = 255$ equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment} \tag{10.8}$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have
: 8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 10.1 gives the resolution for 6-16 bit DACs.

Table 10.1 Resolution for 6–16 bit DACs

Bits	Intervals	LSB size (% of Full Scale)	LSB size (10 V Full Scale)
6	63	1.588%	158.8 mV
8	256	0.392%	39.2 mV
10	1023	0.0978%	9.78 mV
12	4095	0.0244%	2.44 mV
14	16383	0.0061%	0.61 mV
16	65535	0.0015%	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 10.17. The static performance of a DAC is determined by

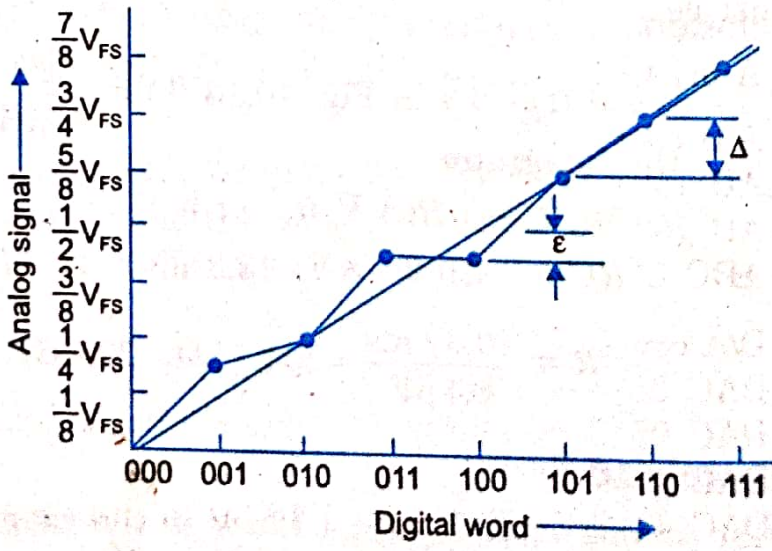

Fig. 10.17 Linearity error for 3-bit DAC

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fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted line and is given by ε/Δ as shown in Fig. 10.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 10.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ± (1/2) LSB at each output level.

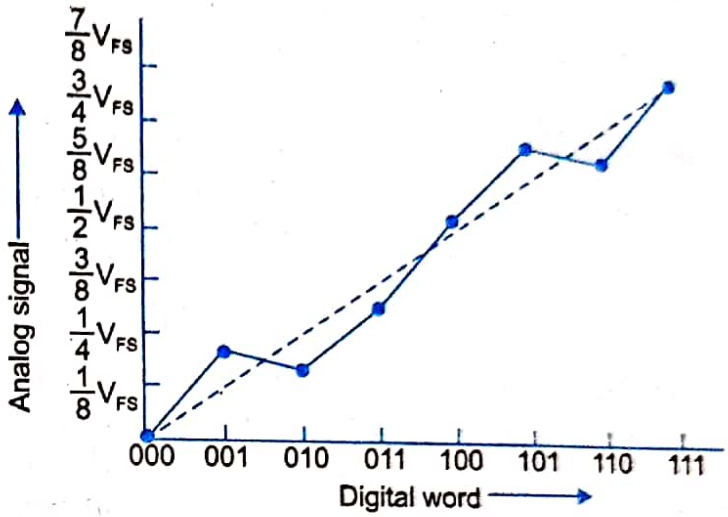

Fig. 10.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:

AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC

D/A converters:

DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

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